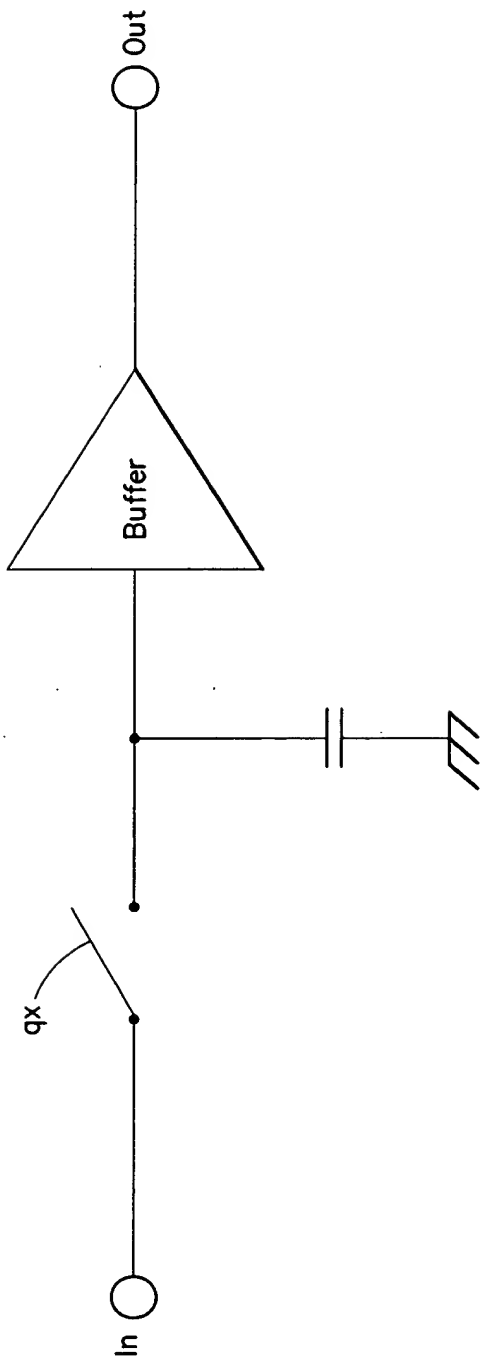


FIG. 1

(Prior Art)



Sample-and-Hold (S/H) Circuit

FIG. 2
(Prior Art)

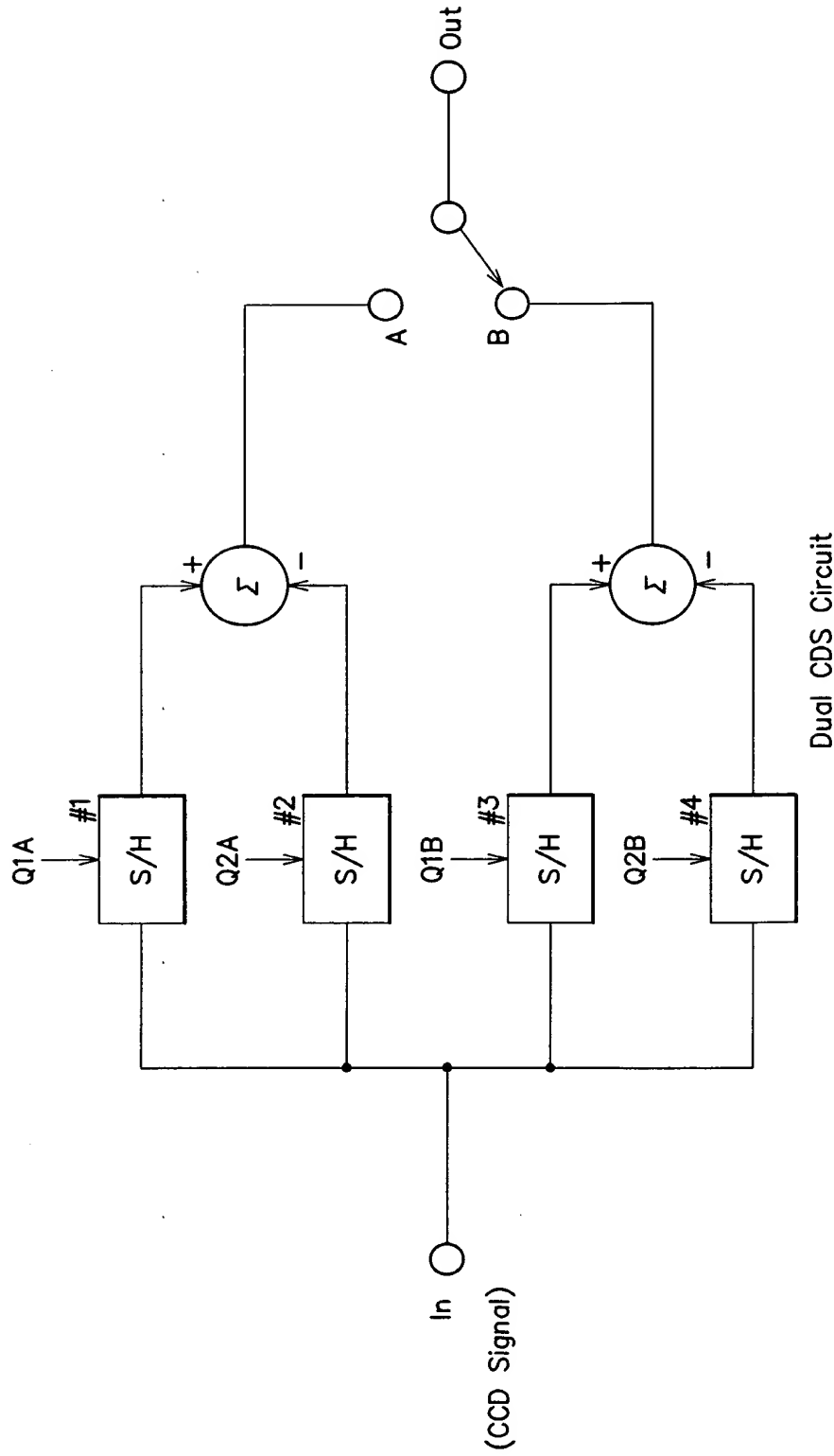


FIG. 3
(Prior Art)

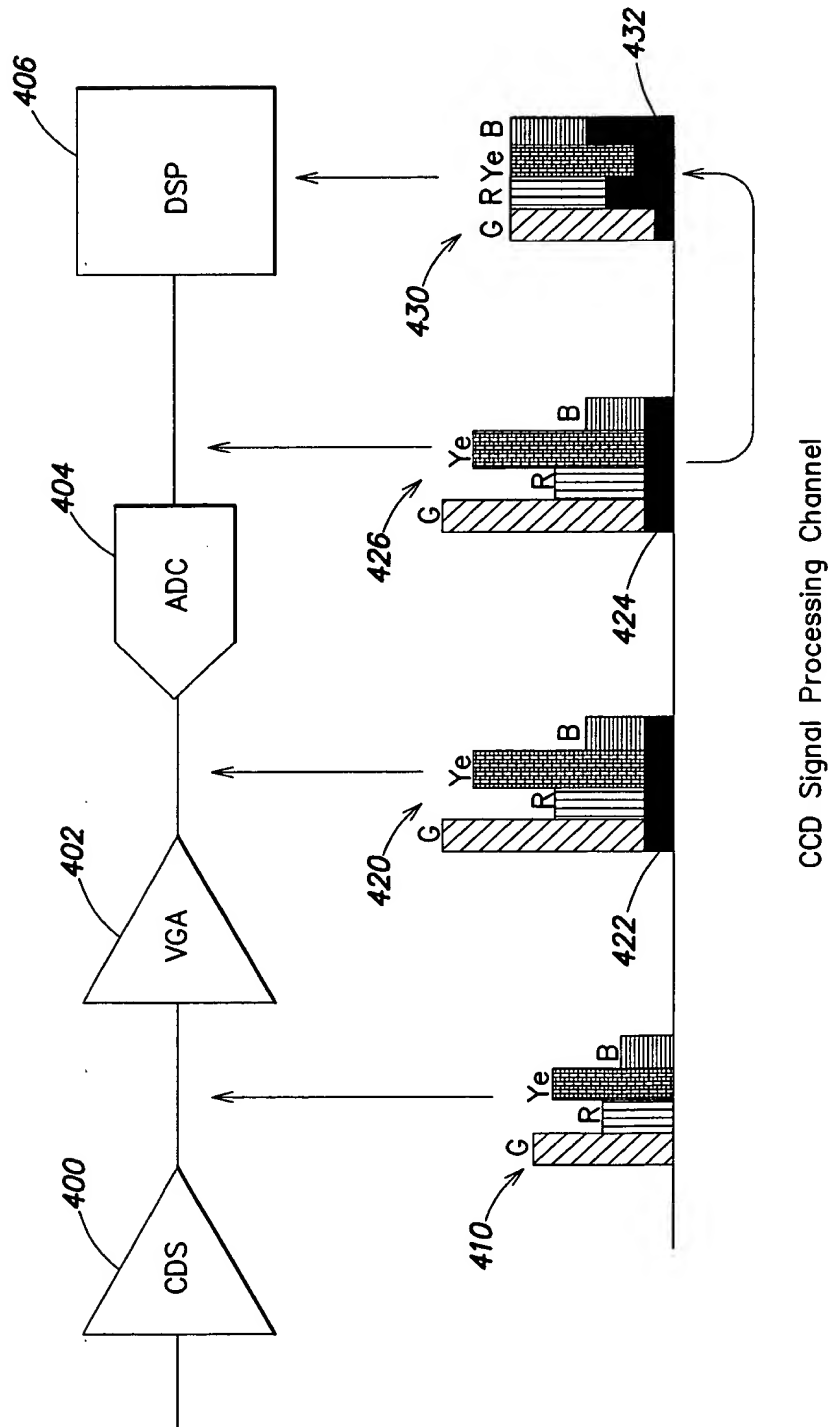


FIG. 4
(Prior Art)

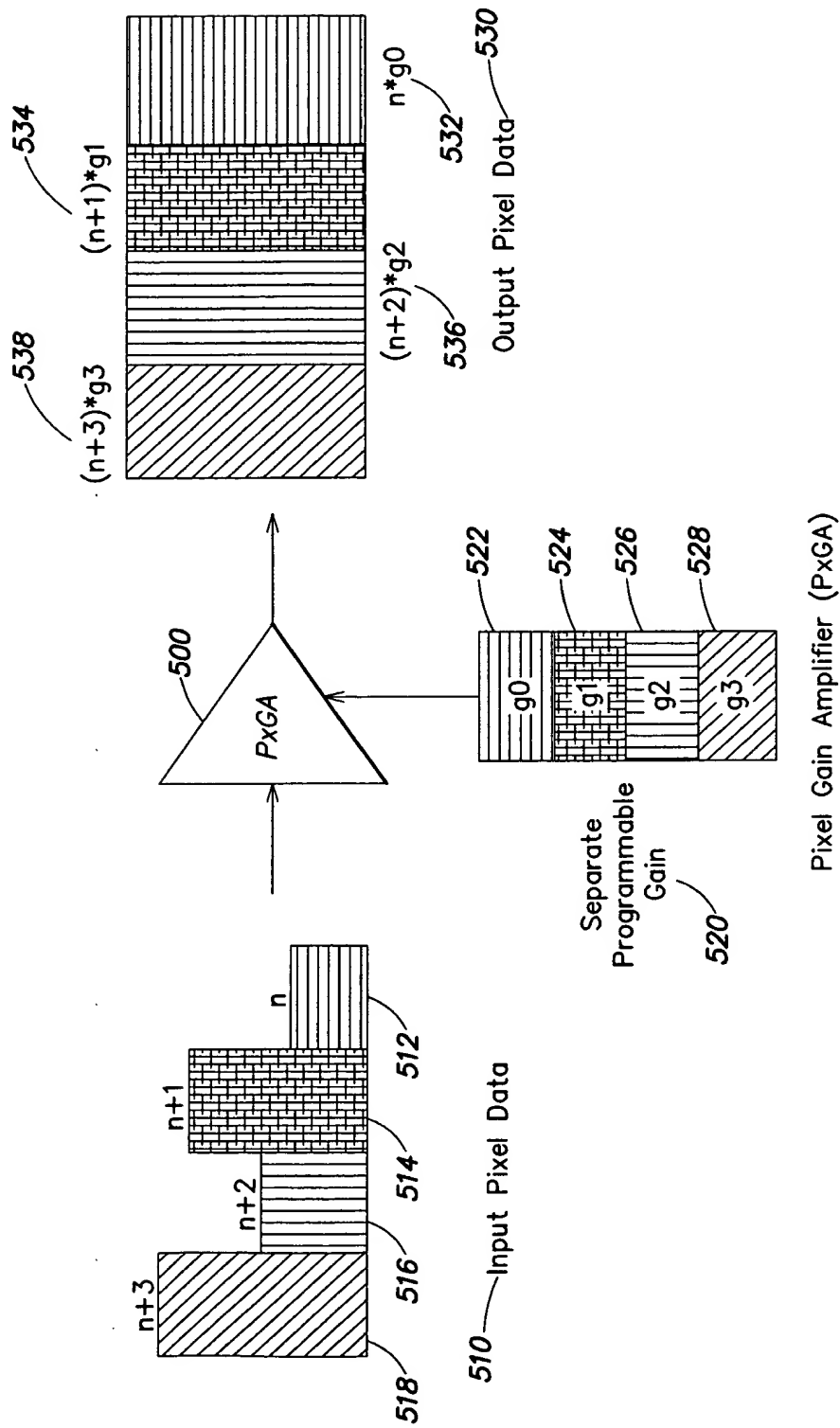
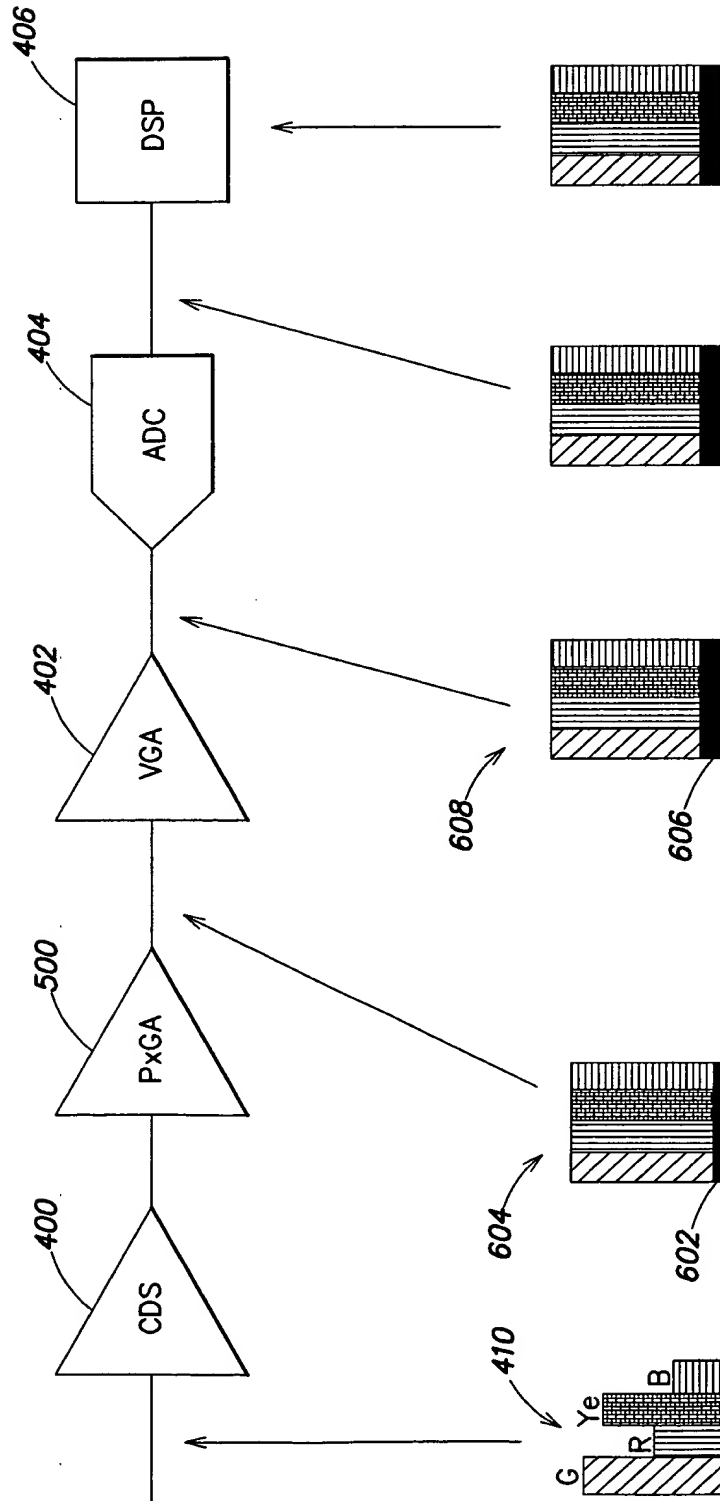


FIG. 5



CCD Signal Processing Channel with PxGA

FIG. 6

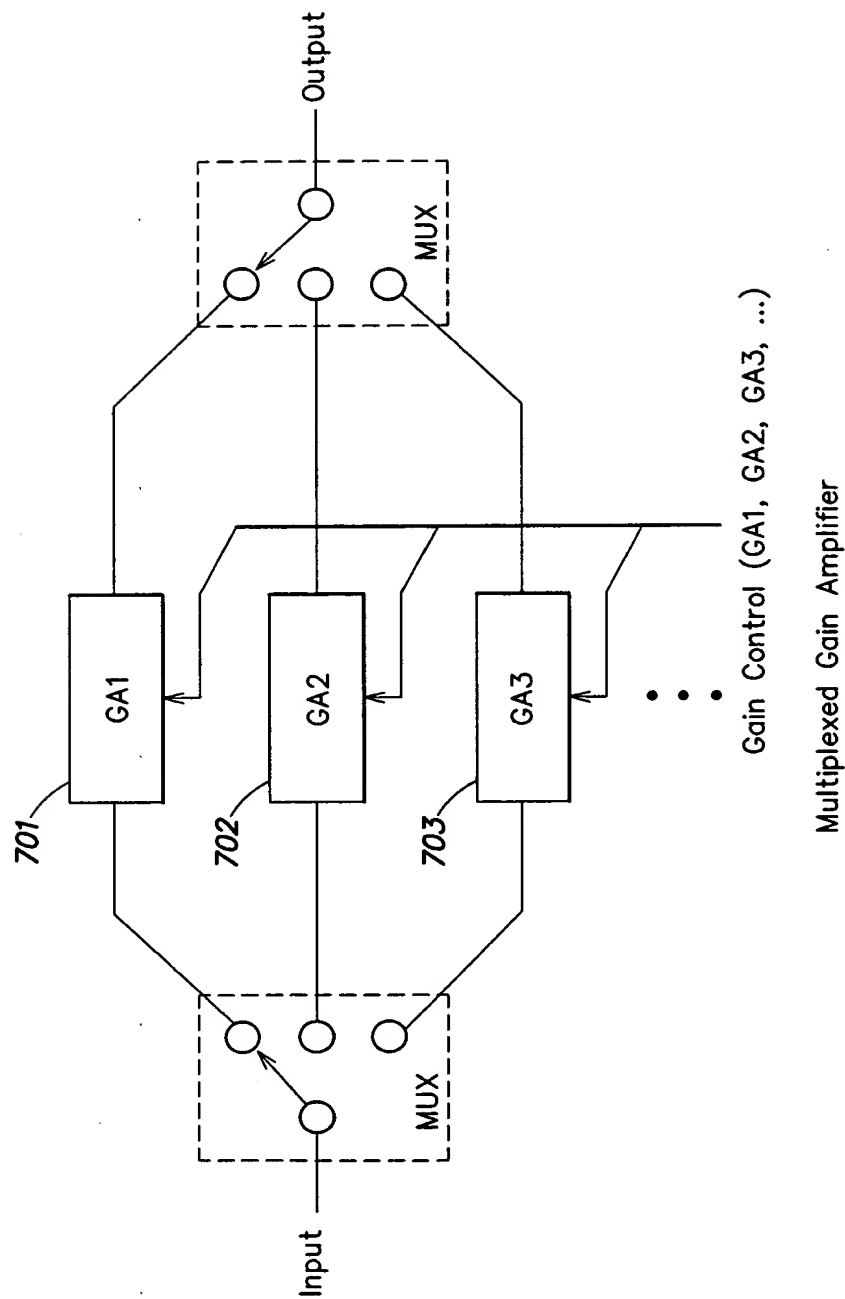


FIG. 7
(Prior Art)

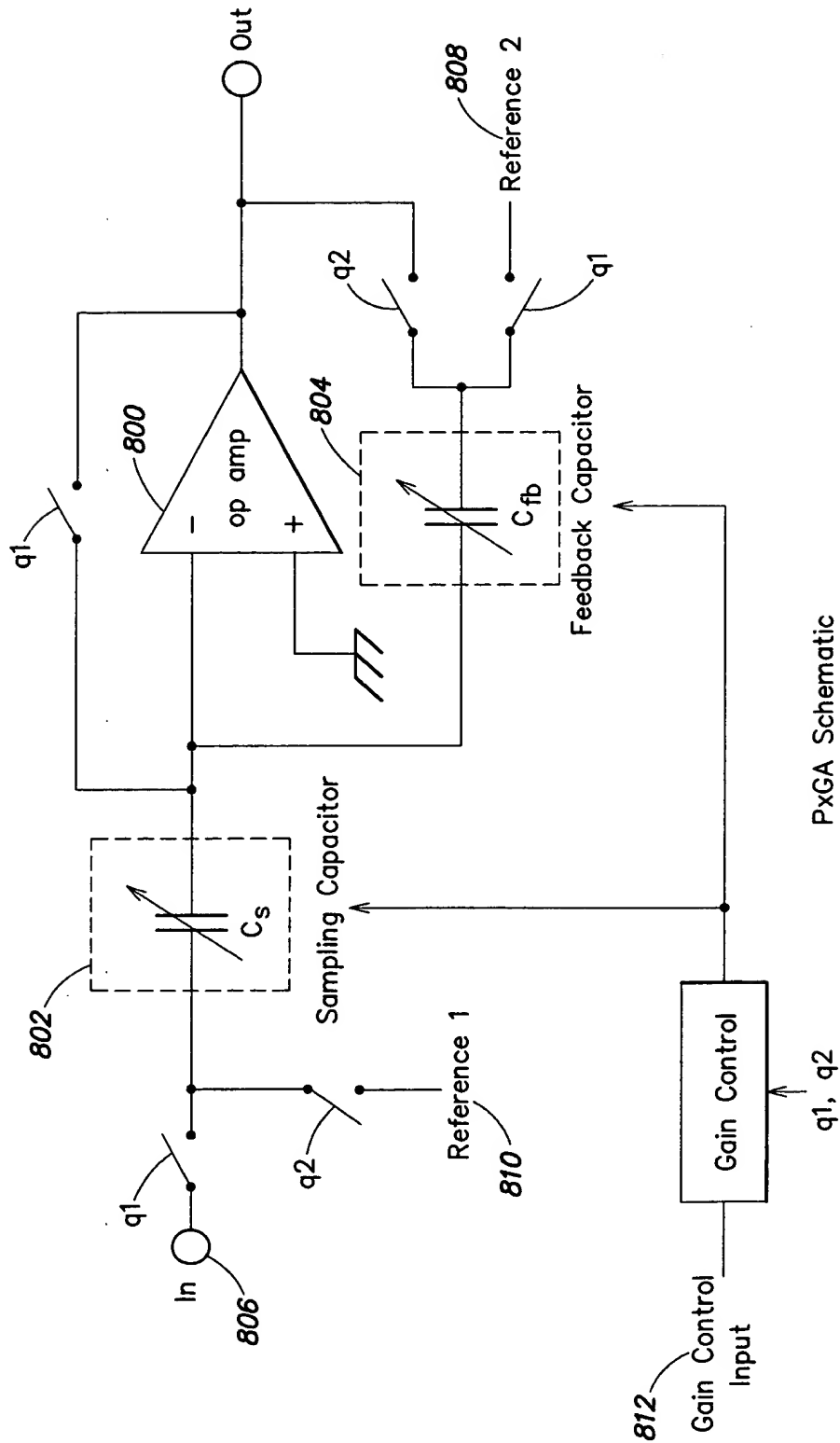


FIG. 8(a)

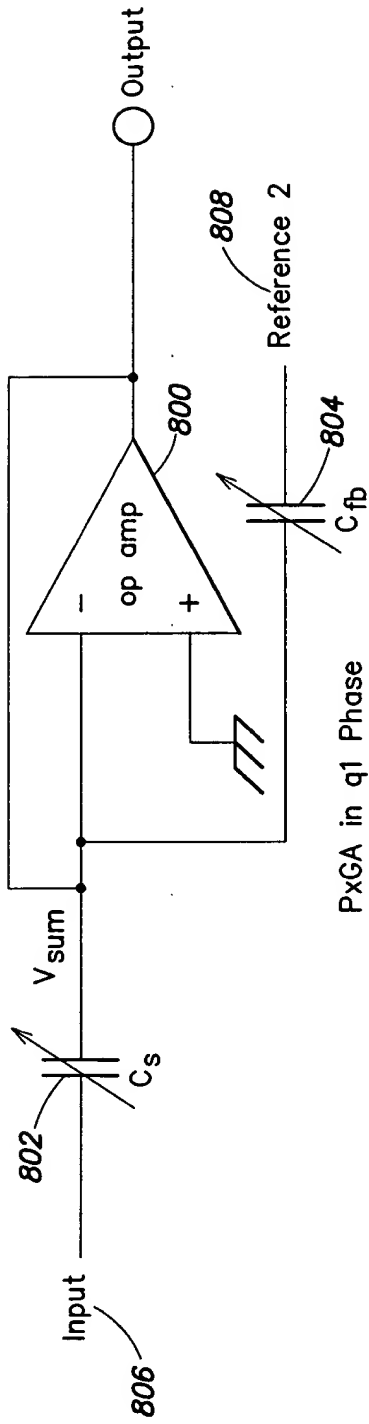


FIG. 8(b)

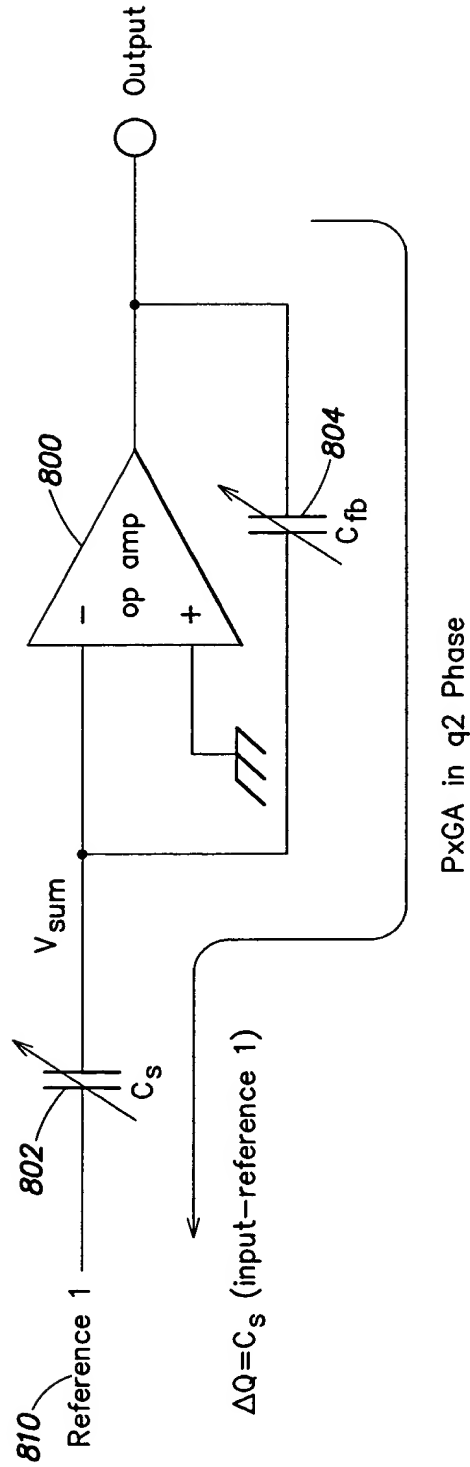
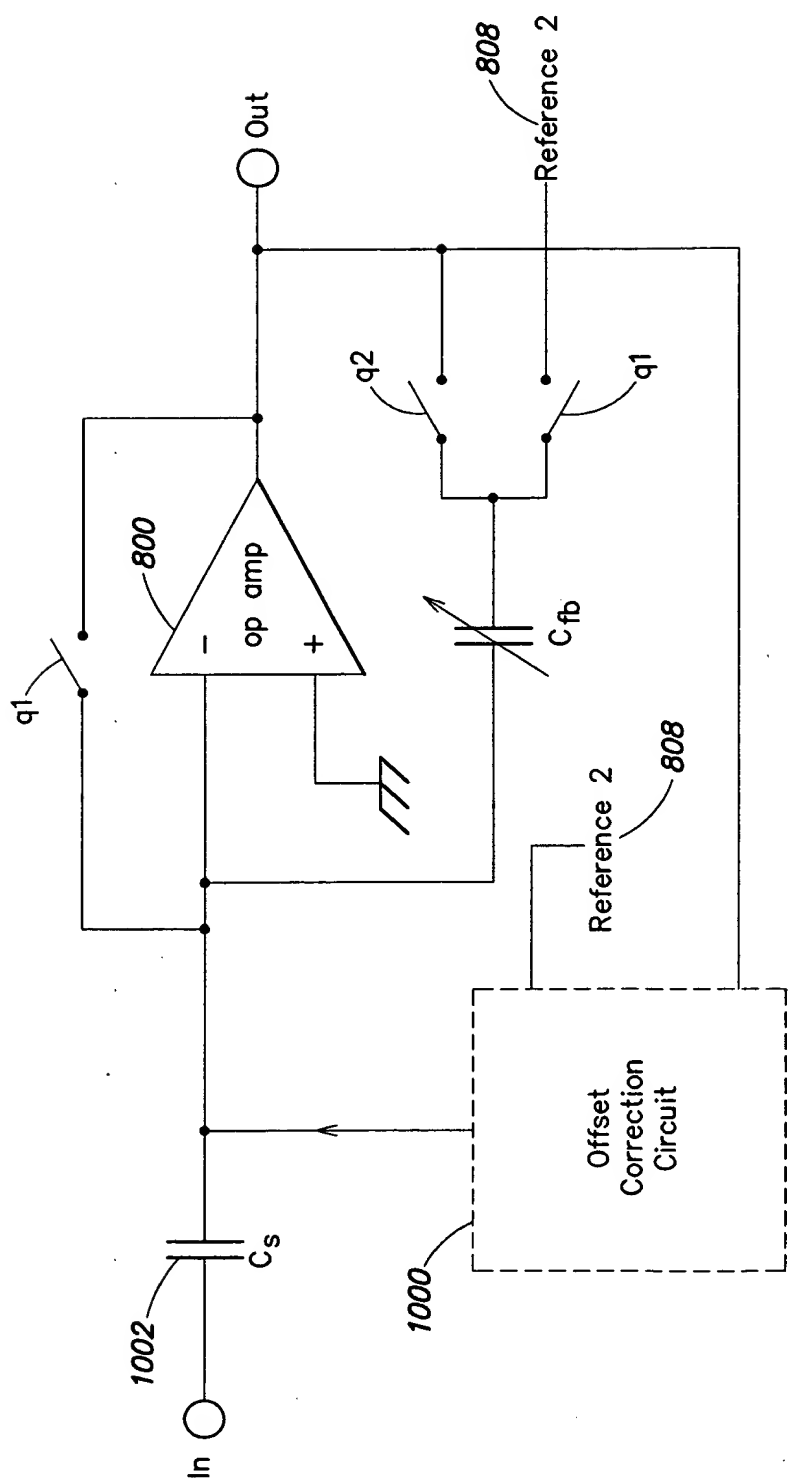


FIG. 8(c)





CDS/PxGA Circuit with Offset Correction

FIG. 10

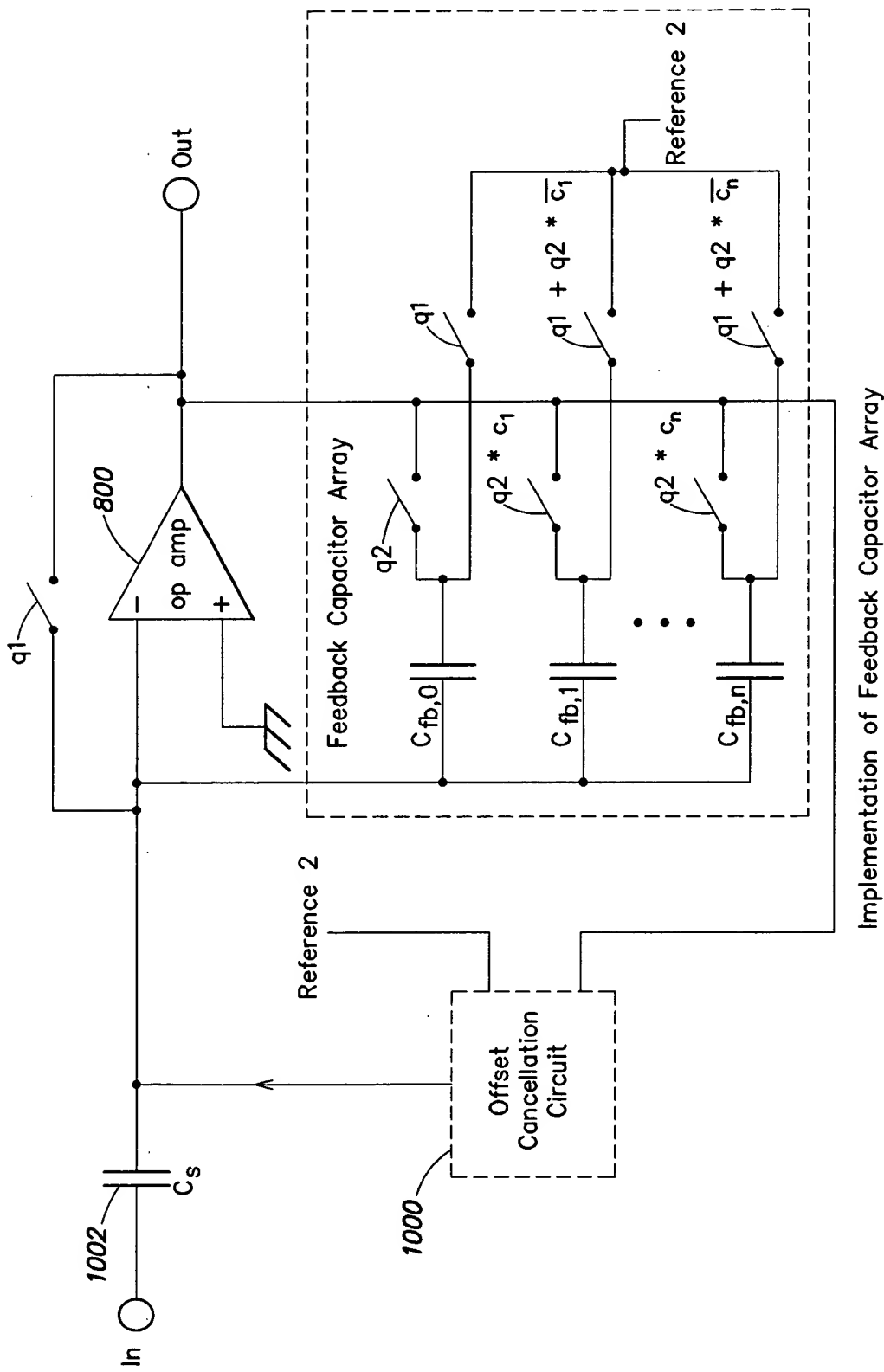


FIG. 11